

What is claimed is:

1. An array of nonvolatile memory cells arranged in a plurality of rows and columns comprising:
- 5 a wordline associated with each row of the array;
- a bitline associated with each column of the array;
- a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with one row and one column in the array, each nonvolatile memory transistor having a source, a drain, a floating gate and a control gate, the control gate of each nonvolatile memory transistor coupled to the one of
- 10 said wordlines with which its row is associated, the drain of each nonvolatile memory transistor coupled to the one of said bitlines with which its column is associated; the source of each nonvolatile memory transistor in a row of the array coupled together; and
- a source transistor associated with each row of the array each said
- 15 source transistor having a gate coupled to the one of said wordlines with which its row is associated, a source coupled to a source potential line, and a drain coupled to the sources of each nonvolatile memory transistor with which its row is associated.

2. The array of claim 1, further comprising disposing said array in an isolation well.

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3. The array of claim 3, further comprising a well selection transistor
5 coupled to said isolation well.

See Fig 2
4. An array of nonvolatile memory cells arranged in a plurality of rows and columns further comprising:

a wordline associated with each row of the array;

10 a bitline associated with each column of the array;

a plurality of split-gate nonvolatile memory transistors, each of said split-gate nonvolatile memory transistors associated with one row and one column in the array, each split-gate nonvolatile memory transistor having a source, a drain, a floating gate and a control gate, the control gate of each split-gate nonvolatile
15 memory transistor coupled to the one of said wordlines with which its row is associated, the drain of each split-gate nonvolatile memory transistor coupled to the one of said bitlines with which its column is associated; the source of each split-gate

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nonvolatile memory transistor in adjacent pairs of rows of the array coupled together; and

a source transistor associated with each row of the array each said source transistor having a gate coupled to the one of said wordlines with which its row is associated, a source coupled to a source potential line, and a drain coupled to the sources of each nonvolatile memory transistor with which its row is associated.

5. The array of claim 4, further comprising disposing said array in an isolation well.

6. The array of claim 5 further comprising a well selection transistor coupled to said isolation well.

See A3
7. An array of one-time programmable nonvolatile memory cells arranged in a plurality of rows and columns comprising:

a wordline associated with each row of the array;

a bitline associated with each column of the array;

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a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with one row and one column in the array, each nonvolatile memory transistor having a source, a drain, and a floating gate, the source of each nonvolatile memory transistor coupled to the one of said wordlines
5 with which its row is associated, the drain of each nonvolatile memory transistor coupled to the one of said bitlines with which its column is associated; and

10 a source transistor associated with each row of the array each said source transistor having a gate coupled to the one of said wordlines with which its row is associated, a source coupled to a source potential line, and a drain coupled to the sources of each nonvolatile memory transistor with which its row is associated.

8. The array of claim 7, further comprising disposing said array in an isolation well.

15 9. The array of claim 8, further comprising a well selection transistor coupled to said isolation well.